

2048 BIT ERASABLE AND ELECTRICALLY REPROGRAMMABLE READ ONLY MEMORY

- Access Time — 1.3 μ sec Max.
- Fast Programming — 2 Minutes for All 2048 Bits
- Fully Decoded, 256 x 8 Organization
- Static MOS — No Clocks Required
- Inputs and Outputs TTL Compatible
- Three-State Output — OR-Tie Capability
- Simple Memory Expansion Chip Select Input Lead

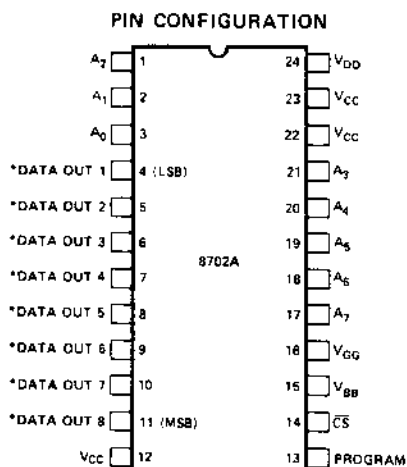
The 8702A is a 256 word by 8 bit electrically programmable ROM ideally suited for microcomputer system development where fast turn-around and pattern experimentation are important. The 8702A undergoes complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.

The 8702A is packaged in a 24 pin dual-in line package with a transparent quartz lid. The transparent quartz lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. This procedure can be repeated as many times as required.

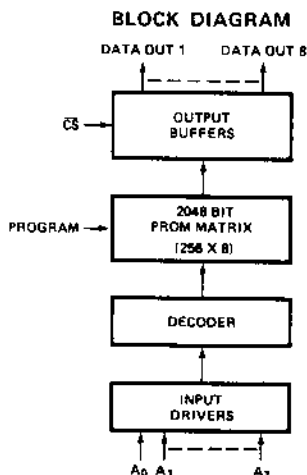
The circuitry of the 8702A is entirely static; no clocks are required.

A pin-for-pin metal mask programmed ROM, the Intel 8302, is ideal for large volume production runs of systems initially using the 8702A.

The 8702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.



*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING.



PIN NAMES

A ₀ -A ₇	ADDRESS INPUTS
CS	CHIP SELECT INPUT
DO ₁ , DO ₂	DATA OUTPUTS

SILICON GATE MOS 8702A

PIN CONNECTIONS

The external lead connections to the 8702A differ, depending on whether the device is being programmed⁽¹⁾ or used in read mode. (See following table.)

MODE \ PIN	12 (V _{CC})	13 (Program)	14 (\overline{CS})	15 (V _{BB})	16 (V _{GG})	22 (V _{CC})	23 (V _{CC})
Read	V _{CC}	V _{CC}	GND	V _{CC}	V _{GG}	V _{CC}	V _{CC}
Programming	GND	Program Pulse	GND	V _{BB}	Pulsed V _{GG} (V _{IL4P})	GND	GND

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +125°C
Soldering Temperature of Leads (10 sec)	+300°C
Power Dissipation	2 Watts
Read Operation: Input Voltages and Supply	
Voltages with respect to V _{CC}	+0.5V to -20V
Program Operation: Input Voltages and Supply	
Voltages with respect to V _{CC}	-48V

* COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V±5%, V_{DD} = -9V±5%, V_{GG}⁽²⁾ = -9V±5%, unless otherwise noted.

SYMBOL	TEST	MIN.	TYP ⁽³⁾	MAX.	UNIT	CONDITIONS
I _{LI}	Address and Chip Select Input Load Current			10	μA	V _{IN} = 0.0V
I _{LO}	Output Leakage Current			10	μA	V _{OUT} = 0.0V, \overline{CS} = V _{CC} - 2
I _{DD0}	Power Supply Current		5	10	mA	V _{GG} = V _{CC} , \overline{CS} = V _{CC} - 2 I _{OL} = 0.0mA, T _A = 25°C
I _{DD1}	Power Supply Current		35	50	mA	\overline{CS} = V _{CC} - 2 I _{OL} = 0.0mA, T _A = 25°C
I _{DD2}	Power Supply Current		32	46	mA	\overline{CS} = 0.0 I _{OL} = 0.0mA, T _A = 25°C
I _{DD3}	Power Supply Current		38.5	60	mA	\overline{CS} = V _{CC} - 2 I _{OL} = 0.0mA, T _A = 0°C
I _{CF1}	Output Clamp Current		8	14	mA	V _{OUT} = -1.0V, T _A = 0°C
I _{CF2}	Output Clamp Current			13	mA	V _{OUT} = -1.0V, T _A = 25°C
I _{GG}	Gate Supply Current			10	μA	
V _{IL1}	Input Low Voltage for TTL Interface	-1.0		0.65	V	
V _{IL2}	Input Low Voltage for MOS Interface	V _{DD}		V _{CC} - 6	V	
V _{IH}	Address and Chip Select Input High Voltage	V _{CC} - 2		V _{CC} + 0.3	V	
I _{OL}	Output Sink Current	1.6	4		mA	V _{OUT} = 0.45V
V _{OL}	Output Low Voltage			0.45	V	I _{OL} = 1.6mA
V _{OH}	Output High Voltage	3.5			V	I _{OH} = -200 μA

Note 1: In the programming mode, the data inputs 1-8 are pins 4-11 respectively, \overline{CS} = GND.

Note 2: V_{GG} may be clocked to reduce power dissipation. In this mode average I_{DD} increases in proportion to V_{GG} duty cycle. (See p. 5)

Note 3: Typical values are at nominal voltages and T_A = 25°C.